Our Docket No.: 0325.00364

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Michael T. Moore et al		
Application No.:	09/605,503	Examiner:	Malzahn, D.
Filed:	June 28, 2000	Art Group:	2124
For:	METHOD OF IMPLEMENTING LOGIC FUNCTIONS USING A LOOK-UP-TABLE		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 1, 2003.

By: Mary Donna Berkley

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-20.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on July 3, 2003. On August 27, 2003, Appellants filed an Amendment After Final and requested reconsideration of the claims. On September 23, 2003, an Advisory Action was issued by the Examiner indicating that (i) the claim amendments would be entered for the purposes of appeal and (ii) the claims remained rejected. On October 3, 2003, Appellants filed a Notice of Appeal.

V. SUMMARY OF INVENTION

The present invention concerns an apparatus generally comprising a first look-up-table (102b), a second look-up-table (102c) and a logic circuit (104). The first look-up-table may

be configured to generate a first partial product signal (RESULTb) from a first address formed by concatenating a first input signal (INa) and a second input signal (INd). The second look-up-table may be configured to generate a second partial product signal (RESULTc) from a second address formed by concatenating a third input signal (INb) and a fourth input signal (INc). The logic circuit may be configured to generate an output signal (OUT) in response to the first partial product signal and the second partial product signal. The first look-up-table and the second look-up-table may be implemented within a multiport memory.

VI. ISSUES

The first issue is whether claims 7-11 are patentable under 35 U.S.C. §112, second paragraph.

The second issue is whether claims 1-11 and 13-20 are patentable under 35 U.S.C. §102(b) over White, U.S. Patent No. 4,344,151.

The third issue is whether claim 12 is patentable under 35 U.S.C. §103(a) over White in view of Chehrazi et al., U.S. Patent No. 6,353,843 (hereafter Chehrazi).

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1, 4, 14 and 15 stand together

Group 2: Claim 2 stands alone.

Group 3: Claim 3 stands alone.

Group 4: Claim 5 stands alone.

Group 5: Claims 6 and 17 stand together.

Group 6: Claims 7, 8 and 9 stand together

Group 7: Claims 10 and 11 stand together.

Group 8: Claim 12 stands alone.

Group 9: Claims 13, 16, 18, 19 and 20 stand together.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other group.

VIII. ARGUMENTS

A. Selected groupings of claims are each patentable under 35 U.S.C.§ 112.

35 U.S.C.§ 112

1. Group 6 (claims 7, 8 and 9) is patentable under 35 U.S.C.§ 112, second paragraph.

The Examiner rejected the claims of group 6 "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."[1] However, the Examiner failed to provide any evidence or argument that the claim language was either (i) indefinite and/or (ii) not the subject matter that the Appellants regard as the invention.[2] Instead, the Examiner asserted that "[t]he concatenating of first and fourth input signals

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[1] Office Action, July 3, 2003, page 3, section 5, lines 1-3

[2] Office Action, July 3, 2003, page 3, section 5

for addressing the third loop-up table is mis-descriptive, note Fig. 1"[3] Mis-descriptive does not appear to be a valid argument for a 35 U.S.C. §112, second paragraph rejection.[4] Therefore, the Examiner has failed to establish that the claims of group 6 are not in compliance with 35 U.S.C. §112, second paragraph for lack of evidence or arguments.

Assuming, *arguendo*, that the Examiner intended the "mis-descriptive" argument to be an indefinite argument (for which Appellants' representative does not necessarily agree), the claims of group 6 are still descriptive relative to FIG. 1 of the application. In particular, the claims of group 6, through dependency on claim 1, provide (i) a first look-up-table (LUT) configured to generate a first partial product signal from a first address formed by concatenating a first input signal and (ii) a second input signal and a second look-up-table configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal. FIG. 1 of the application shows an example implementation of an apparatus with four look-up tables 102a-102n and four signals INa, INb, INc and INd. One of ordinary skill in the art would understand that the four input signals of the claims may be illustrated, for example, by the four signals INa, INb, INc and INd. Therefore, the claimed first and the second look up-tables may be illustrated by either (i) the LUT 102b and LUT 102c or (ii) the LUT 102n and LUT 102a.

Claim 7 provides a third look-up-table configured to generate a third partial product signal from a third address formed by concatenating the first input signal and the fourth input signal. Using the example where the claimed first look-up-table is illustrated by the LUT 102b and the

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[3] Office Action, July 3, 2003, page 3, section 5, lines 4-5.

[4] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, § 2171.

claimed second look-up-table is illustrated by the LUT 102c, the claimed first, second, third and fourth input signals may be illustrated by the signals INa, INd, INb and INc, respectively. Thus, the claimed third look-up-table may be illustrated by the LUT 102b with the claimed first and fourth input signals being illustrated by the signals INa and INc, respectively. Therefore, claim 7 is not mis-descriptive as asserted by the Examiner.[5]

Claim 8 provides a fourth look-up table configured to generate a fourth partial product signal from a fourth address formed by concatenating the second input signal and the third input signal. The fourth claimed look-up-table may be illustrated by the LUT 102a with the claimed second and third input signals being illustrated by the signals INd and INb, respectively. Therefore, the claim 8 is not mis-descriptive as asserted by the Examiner.[6] As such, the claims of group 6 are fully compliant with 35 U.S.C. §112, second paragraph and the rejection should be reversed.

2. **Group 7 (claims 10 and 11) is patentable under 35 U.S.C.§ 112, second paragraph.**

The Examiner rejected the claims of group 6 "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."[7] However, the Examiner failed to provide any evidence or argument that the claim language was either (i) indefinite and/or (ii) not the subject matter that the Appellants regard as the

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[5] Office Action, July 3, 2003, page 3, section 5, lines 4-5

[6] Office Action, July 3, 2003, page 3, section 5, line 8

[7] Office Action, July 3, 2003, page 3, section 5, lines 1-3.

invention.[7] Instead, the Examiner asserted that "[c]laim 10 is mis-descriptive because the first partial product signal is not shifted, note the equation on page 8, line 3."[8] This descriptive does not appear to be a valid argument for a 35 U.S.C. §112, second paragraph rejection.[9] Therefore, the Examiner has failed to establish that the claims of group 7 are not in compliance with 35 U.S.C. §112, second paragraph for lack of evidence or arguments.

Assuming, *arguendo*, that the Examiner intended the "mis-descriptive" argument to be an indefinite argument (for which Appellants' representative does not necessarily agree), the claims of group 7 are still descriptive relative to the equation on page 8, line 3 of the application. In particular, the claims of group 7 provide shifting a first partial product signal. Using the above example (group 6) where the claimed first look-up-table is illustrated by the LUT 102b in FIG. 1 of the application, the claimed first partial product signal may be illustrated by the signal RESULTb generated from the input signals INa and INd. The equation on page 8, line 3 of the application shows shifting of the partial product signal RESULTb by way of an example multiplication (e.g., "*") of A time D (e.g., A.D) that has been shifted (e.g., A.D0). The same multiplication and shift is also illustrated on page 7, lines 13-21 of the application as follows.

```
      AB
    *CD
    ----
      D.B
     A.D
     C.B
   C.A
   ------
   RESULT
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[7] Office Action, July 3, 2003, page 3, section 5

[8] Office Action, July 3, 2003, page 3, section 5, lines 5-6.

[9] M.P.E.P., Eighth Edition, Revised February 2003, §2171

Where the arrows ">>" may represent logical shifts and the "*" may indicate multiplication.

Therefore, claim 10 is not mis-descriptive as asserted by the Examiner[11]. As such, the claims of group 7 are fully compliant with 35 U.S.C. §112, second paragraph and the rejection should be reversed.

B. **Selected groupings of claims are each patentable over White.**

35 U.S.C. § 102

The Federal Circuit has stated that "[t]o anticipate, *every element and limitation* of the claimed invention must be found in a single prior art reference, *arranged as in the claim.*"[12] (Emphasis added). The Federal circuit has added that the anticipation determination is viewed from one of ordinary skill in the art: "There must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[13] Furthermore, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[14]

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[11] Office Action, July 3, 2003, page 3, section 5, lines 5-6.

[12] *Brown v. 3M*, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) citing *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383, 58 USPQ2d 1286, 1291 (Fed. Cir. 2001); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q 2d 1001, 1010 (Fed. Cir. 1991) (Emphasis added by Appellant).

[13] *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991).

[14] *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, USPQ2d 1051, 1053 (Fed Cir. 1987)

1. **Group 1 (claims 1, 4, 14 and 15) is not anticipated by White**

The claims of group 1 provide a first look-up table operation to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal. In contrast, White appears to be silent regarding any memory element 21-28 utilizing an address formed by *concatenating* two input signals. In particular, column 4, line 17 of White states that elements 15, 16, 17 and 18 are *summing means* for the addresses Ar, Br, Ai and Bi. A common definition for a "sum" is "the result of an addition."[15] However, a "concatenation of two strings *a* and *b* is the string *ab* formed by joining *a* and *b*."[16] From the common definitions, one of ordinary skill in the art would understand a summation to be a different operation than a concatenation. Therefore, White does not appear to disclose or suggest a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal as presently claimed.

The claims of group 1 further provide a multiport memory. The United States Patent and Trademark Office defines a "multiport memory" in class 711, subclass 149 as:

> Subject matter including means or steps for controlling *shared memory* capable of supporting a plurality of simultaneous read accesses. (Emphasis added)

One of ordinary skill in the art would not recognize the independent memory elements 21-28 of White, each having a single address input and a single data output, to form a shared memory of a conventional multiport memory. For example, the memory element 21 of White cannot be accessed

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[15] Amendment After Final, August 27, 2003, Appendix A, definition of "sum" from *Eric Weisstein's World of Mathematics*.

[16] Amendment After Final, August 27, 2003, Appendix B, definition of "concatenation" from *Eric Weisstein's World of Mathematics*.

through the address Bi. Therefore, White does not appear to disclose or suggest a multiport memory as presently claimed.

The claims of group 1 further provide generating an output signal in response to the first partial product signal and the second partial product signal. Assuming, *arguendo*, that (i) the memory element 26 of White is similar to the claimed second look-up table and (ii) the output signal of element 41 in FIG. 1 of White is similar to the claimed output signal as asserted by the Examiner[17] (for which Appellants' representative does not necessarily agree), the output signal from element 41 of White does not appear to be generated in response to the signal generated by the memory 26 of White. In particular, the output signal from memory 26 is received by element 32 and the output of element 32 is directed to element 42 of White. Therefore, *prima facie* anticipation has not been established for lack of evidence that the signals and elements of White are arranged as in the claims of group 1.

The claims of group 1 further provide four input signals. In contrast, the Examiner only cites three address signals (Br, Ar and Ai) from White in rejecting the four claimed input signals.[18] Assuming, *arguendo*, that the signal Bi of White is similar to the claimed fourth input signal (for which the Appellants' representative does not necessarily agree), the signal Bi of White does not appear to contribute to the input address for memories 25 or 26, which were asserted by the Examiner to be similar to the claimed first and second look-up-tables.[19] Therefore, the Examiner has

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[17] Office Action, July 3, 2003, page 2, section 2, lines 5 and 7

[18] Office Action, July 3, 2003, page 2, section 2, lines 3-7

[19] Office Action, July 3, 2003, page 2, section 2, lines 3 and 5.

failed to establish *prima facie* anticipation for lack of evidence that the addresses and memory elements of White are arranged as in the group 1 claims.

In summary, the Examiner has failed to establish that White discloses or suggests (i) concatenating two input signals and (ii) a multiport memory. The Examiner has also failed to establish *prima facie* anticipation for (i) generating an output signal in response to the first partial product signal and the second partial product signal and (ii) four input signals concatenated into two look up tables. As such, the claims of group 1 are fully patentable over the cited reference and the rejection should be reversed.

2. Group 2 (claim 2) is not anticipated by White

Claim 2 depends from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 2.

Claim 2 further provides that the multiport memory comprises a dual port memory. In contrast, White appears to be silent regarding dual port memories. Therefore, White does not appear to disclose or suggest a multiport memory comprising a dual port memory as presently claimed.

Furthermore, the Examiner has failed to provide any evidence of anticipation for the claimed dual port memory.[20] Therefore, the Examiner has failed to establish *prima facie* anticipation that a multiport memory comprising a dual port memory is expressly or inherently described by

[20] Office Action, page 2, section 2.

White. As such, claim 2 is fully patentable over the cited reference and the rejection should be reversed.

3. Group 3 (claim 3) is not anticipated by White

Claim 3 depends from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 3.

Claim 3 further provides that the multiport memory comprises a quad port memory. In contrast, White appears to be silent regarding quad port memories. Therefore, White does not appear to disclose or suggest a multiport memory comprising a quad port memory as presently claimed.

Furthermore, the Examiner has asserted that the complex multiplier of White has four input signals and thus constitutes a quad port memory. However, none of the four addresses Ar, Br, Ai and Bi of White appear to be able to access all of the memory elements 21-28 as would be the case in a conventional quad port memory. For example, address Ar cannot access the contents of memory element 22. Instead, White appears to disclose nothing more than eight independent single port memory elements each receiving information from at most two address among the four addresses Ar, Br, Ai and Bi. Therefore, the Examiner has failed to establish *prima facie* anticipation that a quad port memory is expressly or inherently described by White. As such, claim 3 is fully patentable over the cited reference and the rejection should be reversed.

4. Group 4 (claim 5) is not anticipated by White

Claim 5 depends from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 4.

Claim 5 further provides a first input signal that is substantially equal to one of a third input signal and a fourth input signal. In contrast, White appears to be silent regarding using a substantially equal signal for two addresses into two of the memory elements 21-28. In particular, FIGS. 1-6 of White appear to disclose that the address received by each memory element 21-28 is unique. Therefore, White does not appear to disclose or suggest a first input signal that is substantially equal to one of a third input signal and a fourth input signal as presently claimed.

Furthermore, the assertion by the Examiner to "note the above paragraph" does not appear to provide any evidence that White discloses or suggests substantially equal input signals.[1] Nothing in page 2, section 2 of the Office Action appears to cite evidence in White for substantially equal inputs. Therefore, the Examiner has failed to establish *prima facie* anticipation that substantially equal inputs are expressly or inherently described by White. As such, claim 5 is fully patentable over the cited reference and the rejection should be reversed.

5. Group 5 (claims 6 and 17) is not anticipated by White

The claims of group 5 depend from the independent claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 5.

[1] Office Action, July 3, 2003, page 2, section 2, line 11.

The claims of group 5 further provide a first input signal that comprises a single-bit serial configuration. In contrast, White appears to be silent regarding a single-bit serial configuration for the addresses Ar, Br, Ai and Bi. Therefore, White does not appear to disclose or suggest a first input signal that comprises a single-bit serial configuration as presently claimed.

Furthermore, the assertion on by the Examiner that "if data is represented as a single bit then there is no difference between a serial and a parallel configuration"[4] does not appear to be expressly or inherently described by White. Since White appears to be silent regarding a single-bit parallel address (an oxymoron in itself), the hypothetical "if" asserted by the Examiner is irrelevant. Therefore, the Examiner has failed to establish *prima facie* anticipation that a single-bit serial configuration is expressly or inherently described by White. As such, the claims of group 5 are fully patentable over the cited reference and the rejection should be reversed.

6. Group 6 (claims 7, 8 and 9) is not anticipated by White

The claims of group 6 depend from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 6.

The claims of group 6 further provide a third look-up-table configured to generate a third partial product signal from a third address formed by concatenating the first input signal and the fourth input signal. In contrast, White appears to be silent regarding concatenating any two of the addresses Ar, Br, Ai or Bi. Therefore, White does not appear to disclose or suggest a third look-

[4] Office Action, July 3, 2003, page 2, section 3, lines 11-13.

up-table configured to generate a third partial product signal from a third address formed by concatenating a first input signal and a fourth input signal as presently claimed.

Furthermore, the Examiner has failed to provide any evidence of anticipation for concatenation of a first input signal and a fourth input signal.[1] Therefore, the Examiner has failed to establish *prima facie* anticipation that a third look-up-table configured to generate a third partial product signal from a third address formed by concatenating a first input signal and a fourth input signal is expressly or inherently described by White. As such, the claims of group 6 are fully patentable over the cited reference and the rejection should be reversed.

7. **Group 7 (claims 10 and 11) is not anticipated by White**

The claims of group 7 depend from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 7.

The claims of group 7 further provide that the logic circuit is further configured to shift the first partial product signal in response to a first shift signal before generating the output signal. In contrast, White appears to be silent regarding shifting any signal presented by the memory elements 21-28. Therefore, White does not appear to disclose or suggest a logic circuit configured to shift a first partial product signal in response to a first shift signal before generating an output signal as presently claimed.

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[1] Office Action, July 3, 2003, page 2, section 2.

Furthermore, the Examiner has failed to provide any evidence of anticipation for shifting.[24] Therefore, the Examiner has failed to establish *prima facie* anticipation that a logic circuit configured to shift a first partial product signal in response to a first shift signal before generating an output signal is expressly or inherently described by White. As such, the claims of group 7 are fully patentable over the cited reference and the rejection should be reversed.

8. Group 9 (claims 13, 16, 18, 19 and 20) is not anticipated by White

The claims of group 9 depend from the independent claims of group 1 and thus contains all of the limitations of group 1. Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 9.

Furthermore, the Examiner has failed to provide any evidence of anticipation for any of the elements within the claims of group 9.[25] Therefore, the Examiner has failed to establish *prima facie* anticipation that the elements for the claims of group 9 are expressly or inherently described by White. As such, the claims of group 9 are fully patentable over the cited reference and the rejection should be reversed.

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[24] Office Action, July 3, 2003, page 2, section 2

[25] Office Action, July 3, 2003, page 2, section 2.

C. Selected groupings of the claims are each patentable over White in view of Chehrazi

35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[26] "[T]he factual inquiry whether to combine references must be thorough and searching."[27] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[28] "It must be based on objective evidence of record."[29] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations as arranged in the claims.[30] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[31]

[26] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[27] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001)

[28] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[29] *Id.* at 1343, 61 USPQ2d at 1434.

[30] M.P.E.P., Eighth Edition, Revised February 2003 §2142

[31] *In re Anita Dembiczak and Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

1. Group 8 (claim 12) is patentable over White in view of Chebrazi

Claim 12 depends from claim 1 and thus contains all of the limitations of claim 1 (group 1). Consequently, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 8.

The Examiner has failed to establish *prima facie* obviousness for lack of clear and particular evidence to combine the White and Chebrazi references. The Examiner has failed to provide particular findings as to the reasons a skilled artisan with no knowledge of the presently claimed invention, would have selected the cited references for combination. The factual inquiry whether to combine references must be thorough and searching. The rigorous application of the requirement for showing the teaching or motivation to combine references is necessary to avoid the subtle but powerful attraction of a hindsight-based obviousness analysis. It is improper, in determining whether a person of ordinary skill in the art would have been led to the combination of references, simply to use that which the inventor taught against its teacher. As such, because of a lack of particular findings as to the reasons a skilled artisan, with no knowledge of the presently claimed invention, would have selected the cited references for combination, the Examiner does not appear to have met the burden of factually establishing a *prima facie* case of obviousness.[1] Therefore, claim 12 is fully patentable over the cited references and the rejection should be reversed.

[1] M.P.E.P., Eighth Edition, Revised February 2003, §2142

Groups 1-9 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[3] As such, each of the above groups is considered to be separately patentable over every other group.[4] In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Group 2 includes an argument that White does not disclose or suggest a dual port memory as presently claimed. Since group 1 does not depend on the dual port memory argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that White does not disclose or suggest a quad port memory as presently claimed. Since groups 1 and 2 do not depend on the quad port memory argument, group 3 may be found patentable even in groups 1 and/or 2 are not.

Group 4 includes an argument that White does not disclose or suggest a first input signal substantially equal to a third input signal or a fourth input signal. Since groups 1-3 do not depend on the substantially equal argument, group 4 may be found patentable even if groups 1, 2 and/or 3 are not.

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[3] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (it is well established that each claim in a patent constitutes a separate invention.).

[4] M.P.E.P., Eighth Edition, Revised February 2003, S1206.

Group 5 includes an argument that White does not disclose or suggest a single-bit serial configuration. Since groups 1-4 do not depend on the single bit serial argument, group 5 may be found patentable even if groups 1-3 and/or 4 are not.

Group 6 includes an argument that White does not disclose or suggest a third look-up-table as presently claimed. Since groups 1-5 do not depend on the third look-up-table argument, group 6 may be found patentable even if groups 1-4 and/or 5 are not.

Group 7 includes an argument that White does not disclose or suggest shifting as presently claimed. Since groups 1-6 do not depend on the shifting argument, group 7 may be found patentable even if groups 1-5 and/or 6 are not.

Group 8 includes an argument that the Examiner has failed to establish *prima facie* obviousness to combine White and Chehrazi. Since groups 1-7 do not depend on the obviousness argument, group 8 may be found patentable even if groups 1-6 and/or 7 are not.

Group 9 includes an argument that the Examiner has failed to provide evidence of anticipation for the claimed elements. Since groups 1-8 do not depend on the lack of evidence argument, group 9 may be found patentable even if groups 1-8 and/or 7 are not.

D. CONCLUSION

None of the cited references concern concatenated input signals or a multiport memory as recited in claims 1, 14 and 15. The Examiner has failed to provide evidence of anticipation for claims 2, 5-11, 13 and 16-20. Furthermore, claims 7-11 are compliance with 35 U.S.C. §112, second paragraph. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the

Examiner's rejection of all pending claims, and hold that the claims are not rendered anticipated or obvious by the cited references. However, should the Board find the arguments herein in support of independent claims 1, 14, and/or 15 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups

Respectfully submitted,

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Docket Number: 0325.00364
Application No.:

IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows.

1. An apparatus comprising:

a first look-up-table configured to generate a first partial product signal from a first address formed by concatenating a first input signal and a second input signal;

a second look-up-table configured to generate a second partial product signal from a second address formed by concatenating a third input signal and a fourth input signal; and

a logic circuit configured to generate an output signal in response to said first partial product signal and said second partial product signal, wherein said first look up-table and said second look up-table are implemented within a multiport memory

2. The apparatus according to claim 1, wherein said multiport memory comprises a dual port memory.

3. The apparatus according to claim 1, wherein said multiport memory comprises a quad port memory.

4. The apparatus according to claim 1, wherein said multiport memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, and a flash memory

5. The apparatus according to claim 1, wherein said first input signal is substantially equal to one of said third input signal and said fourth input signal.

6. The apparatus according to claim 1, wherein said first input signal comprises a single bit serial configuration.

7. The apparatus according to claim 1, further comprising:

a third look-up table configured to generate a third partial product signal from a third address formed by concatenating said first input signal and said fourth input signal.

8. The apparatus according to claim 7, further comprising:

a fourth look-up-table configured to generate a fourth partial product signal from a fourth address formed by concatenating said second input signal and said third input signal.

9. The apparatus according to claim 8, wherein said logic circuit is further configured to generate said output signal in further response to said third partial product signal and said fourth partial product signal.

10. The apparatus according to claim 1, wherein said logic circuit is further configured to shift said first partial product signal in response to a first shift signal before generating said output signal.

11. The apparatus according to claim 10 wherein said logic circuit is further configured to shift said second partial product signal in response to a second shift signal before generating said output signal.

12. The apparatus according to claim 1 further comprising:

a plurality of registers disposed between said first and said second look-up-tables and said logic circuit.

13. The apparatus according to claim 1, wherein said first partial result signal is an arithmetic function of said first input signal and said second input signal.

14. An apparatus comprising:

means for generating a first partial product signal by looking-up a first address formed by concatenating a first input signal and a second input signal to a multiport memory;

means for generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

means generating an output signal in response to said first partial product signal and said second partial product signal.

15. A method for implementing logical functions, comprising the steps of:

(A) generating a first partial product signal by looking up an address formed by concatenating a first input signal and a second input signal to a multiport memory,

(B) generating a second partial product signal by looking-up a second address formed by concatenating a third input signal and a fourth input signal to said multiport memory; and

(C) generating an output signal in response to said first partial product signal and said second partial product signal.

16. The method according to claim 15, wherein said first partial product signal is a logical function of said first input signal and said second input signal.

17. The method according to claim 15, wherein said first input signal has a single-bit serial configuration.

18. The method according to claim 15, wherein said multiport memory is selected from a group consisting of a RAM, a ROM, a PROM, an EPROM, an EEPROM, and a flash memory.

19. The method according to claim 15, wherein step (C) comprises the step of adding said first partial product signal and said second partial product signal.

20. The method according to claim 19, further comprising the step of:

shifting said first partial product signal in response to a first shift signal before adding to said second partial product signal.

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